Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Claims 1-191 (Cancelled).

192. (Previously Presented) Apparatus adapted to be coupled to at least a twisted first wire pair enabling receipt of at least first, second and third discrete analog signal levels with different amplitudes representing information, a twisted second wire pair enabling receipt of at least fourth, fifth and sixth discrete analog signal levels with different amplitudes representing information and a twisted third wire pair enabling receipt of at least seventh, eighth and ninth discrete analog signal levels with different amplitudes representing information, the analog signal levels being received one discrete signal level at a time, the apparatus comprising:

an analog to digital converter arranged to convert the first discrete analog signal level to a corresponding digital first information signal, to convert the second discrete analog signal level to a corresponding digital second information signal, to convert the third discrete analog signal level to a corresponding digital third information signal, to convert the fourth analog signal level to a corresponding digital fourth information signal, to convert the fifth discrete analog signal level to a corresponding digital fifth information signal, to convert the sixth discrete analog signal level to a corresponding digital sixth information signal, to convert the seventh discrete analog signal level to a corresponding digital seventh information signal, to convert the eighth discrete analog signal level to a corresponding digital eighth information signal and to convert the ninth discrete analog signal level to a corresponding digital ninth information signal; and

circuitry arranged to individually identify each of the first, second, third, fourth, fifth, sixth, seventh, eighth and ninth discrete analog signal levels, to shift in time the first information signal relative to the first discrete analog signal level, to shift in time the second information signal relative to the second discrete analog signal level, to shift in time the third information

signal relative to the third discrete analog signal level, to shift in time the fourth information signal relative to the fourth discrete analog signal level, to shift in time the fifth information signal relative to the fifth discrete analog signal level, to shift in time the sixth information signal relative to the sixth discrete analog signal level, to shift in time the seventh information signal relative to the seventh discrete analog signal level, to shift in time the eighth information signal relative to the eighth discrete analog signal level and to shift in time the ninth information signal relative to the ninth discrete analog signal level.

193. (Previously Presented) The apparatus of claim 192 wherein the analog to digital converter is arranged to convert the discrete analog signals levels to corresponding digital information signals at a particular rate and wherein the circuitry comprises a timing recovery circuit arranged to regulate the particular rate at which said analog to digital converter converts the discrete analog signal levels.

194. (Previously Presented) The apparatus of claim 193 wherein the circuitry comprises a digital adaptive equalizer arranged to identify the discrete analog signal level being received on each of the wire pairs.

195. (Previously Presented) The apparatus of claim 194 and further comprising an automatic gain control circuit coupled to the analog to digital converter.

196. (Previously Presented) The apparatus of claim 194 and further comprising a decoder circuit coupled to the digital adaptive equalizer.

197. (Previously Presented) The apparatus of claim 196 and further comprising a media access controller coupled to said decoder circuit.

198. (Previously Presented) The apparatus of claim 194 wherein the digital adaptive equalizer includes a feedforward equalizer, a data slicer and a decision feedback equalizer.

199. (Previously Presented) The apparatus of claim 194 wherein said timing recovery circuit regulates the particular rate in accordance with a product of a plurality of signal samples.

200. (Previously Presented) The apparatus of claim 192 and further comprising a clock arranged to generate clock signals having a phase and wherein the analog to digital converter is arranged to convert the discrete analog signal levels to the corresponding digital information digital signals in response to the clock signals and wherein the circuitry is arranged to shift the phase of the clock signals so that the time at which the analog to digital converter samples the discrete analog signal levels is adjusted.

201. (Previously Presented) The apparatus of claim 200 wherein the circuitry shifts the phase of the clock signals in accordance with a product of a plurality of signal samples.

202. (Previously Presented) The apparatus of claim 200 where each of the wire pairs also enables receipt of timing discrete analog signal levels, wherein the analog to digital converter is arranged to convert the timing discrete analog signal levels to corresponding timing digital signals in response to the clock signals, and wherein the circuitry is arranged to shift the phase of the clock signals in response to the timing digital signals.

203. (Previously Presented) The apparatus of claim 202 wherein the circuitry is arranged to shift the phase of the clock signals in response to both the timing digital signals and the information digital signals.

204. (Previously Presented) In apparatus adapted to be coupled to at least a twisted first wire pair enabling receipt of at least first, second and third discrete analog signal levels with different amplitudes representing information, a twisted second wire pair enabling receipt of at least fourth, fifth and sixth discrete analog signal levels with different amplitudes representing information and a twisted third wire pair enabling receipt of at least seventh, eighth and ninth discrete analog signal levels with different amplitudes representing information, the analog signal levels being received one discrete signal level at a time, a method of processing the received discrete analog signal levels comprising:

converting the first discrete analog signal level to a corresponding digital first information signal;

converting the second discrete analog signal level to a corresponding digital second information signal;

converting the third discrete analog signal level to a corresponding digital third information signal;

converting the fourth discrete analog signal level to a corresponding digital fourth information signal;

converting the fifth discrete analog signal level to a corresponding digital fifth information signal;

converting the sixth discrete analog signal level to a corresponding digital sixth information signal;

converting the seventh discrete analog signal level to a corresponding digital seventh information signal;

converting the eighth discrete analog signal level to a corresponding digital eighth information signal;

converting the ninth discrete analog signal level to a corresponding digital ninth

information signal;

individually identifying each of the first, second, third, fourth, fifth, sixth, seventh, eighth and ninth discrete analog signal levels;

shifting in time the first information signal relative to the first discrete analog signal level;

shifting in time the second information signal relative to the second discrete analog signal level;

shifting in time the third information signal relative to the third discrete analog signal level;

shifting in time the fourth information signal relative to the fourth discrete analog signal level;

shifting in time the fifth information signal relative to the fifth discrete analog signal level;

shifting in time the sixth information signal relative to the sixth discrete analog signal level;

shifting in time the seventh information signal relative to the seventh discrete analog signal level;

shifting in time the eighth information signal relative to the eighth discrete analog signal level; and

shifting in time the ninth information signal relative to the ninth discrete analog signal level.

205. (Previously Presented) The method of claim 204 wherein each of the converting steps comprises converting one of the discrete analog signals levels to a corresponding one of the information signals at a particular rate and further comprising regulating the particular rate.

206. (Previously Presented) The method of claim 205 wherein said regulating comprises regulating the particular rate in accordance with a product of a plurality of signal samples.

207. (Previously Presented) The method of claim 204 and further comprising controlling the gain of the each of the received discrete analog signal levels.

208. (Previously Presented) The method of claim 204 and further comprising decoding each of the digital information signals.

209. (Previously Presented) The method of claim 204 and further comprising controlling media access.

210. (Previously Presented) The method of claim 204 and further comprising generating clock signals having a phase and wherein each of the converting steps comprises converting one of the discrete analog signal levels to one of the corresponding digital information signals in response to the clock signals and wherein each of the shifting steps comprises shifting the phase of the clock signals so that the time at which the converting occurs is adjusted.

211. (Previously Presented) The method of claim 210 wherein the shifting comprises shifting the phase of the clock signals in accordance with a product of a plurality of signal samples.

212. (Previously Presented) The method of claim 210 wherein each of the wire pairs enables receipt of timing discrete analog signal levels, wherein the converting further comprises

converting the timing discrete analog signal levels to corresponding timing digital signals in response to the clock signals, and wherein the shifting further comprises shifting the phase of the clock signals in response to the timing digital signals.

213. (Previously Presented) The method of claim 212 wherein the shifting comprises shifting the phase of the clock signals in response to both the timing digital signals and the digital information signals.

214. (Previously Presented) A communication system for decoding signals having three or more analog signal levels to represent information transmitted by a first computer over a plurality of pairs of twisted wires to a second computer, said communication system including a transceiver comprising:

a plurality of receivers and transmitters operatively coupled to respective ones of said plurality of said pairs of twisted wires, wherein each of said plurality of receivers comprises:

an analog to digital converter;

an automatic gain control circuit; and

a digital adaptive equalizer, said equalizer further comprising a feed forward equalizer, a decision feedback equalizer, and a data slicer;

wherein each of said analog to digital converters sampling said analog signal at a sampling rate, each of said automatic gain control circuits receiving said analog signal from one of said pairs of twisted wires and providing gain control at the input to a respective one of said analog to digital converters, and each of said equalizers producing recovered digital data from said sampled analog signal provided at the input of said equalizer; and

wherein said transceiver also includes a plurality of transmitters that simultaneously transmit three or more analog signal levels to said first computer over said plurality of pairs of twisted wires.

215. (Previously Presented) The system of claim 214, wherein said transceiver combines said recovered data from each of said digital adaptive equalizers into a single recovered digital data stream.

216. (Previously Presented) The system of claim 215, wherein said single recovered data stream is Ethernet data.

217. (Previously Presented) The system of claim 214, wherein said communication system is an Ethernet system.

218. (Previously Presented) The system of claim 214, wherein the digital data is Ethernet data with a data rate of at least 100 Mbps.

219. (Previously Presented) The system of claim 214, wherein each of said equalizer includes an adder that sums the output of respective ones of said decision feedback equalizers and said feed forward equalizers.

220. (Previously Presented) The system of claim 219, wherein the digital data is Ethernet data.

221. (New) A computer network device, comprising:

transmitting circuitry including an encoder and data splitter circuitry, a first transmitter, a second transmitter and a third transmitter, wherein the first transmitter, the second transmitter and the third transmitter are coupled to a network via a respective pair of twisted wires;

receiving circuitry including clock recover circuitry, data combiner and decoder circuitry,

a first receiver and equalizer, a second receiver and equalizer and a third receiver and equalizer, wherein the clock recover circuitry is disposed along a data path between the receivers and equalizers and the data combiner and decoder circuitry, wherein the first receiver and equalizer, the second receiver and equalizer and the third receiver and equalizer is coupled to the network via a respective pair of twisted wires;

a media access control coupled to a system bus, the encoder and data splitter circuitry of the transmitting circuitry and the data combiner and decoder circuitry of the receiver circuitry; and

collision detect and link control circuitry coupled to the media access control, the transmitters and the receivers and equalizers,

wherein the first receiver and equalizer comprises an automatic gain control stage, an analog-to-digital converter and a digital adaptive equalizer, wherein the automatic gain control state is coupled to the analog-to-digital converter, and wherein the analog-to-digital converter is coupled to the digital adaptive equalizer.

222. (New) The computer network device according to claim 221, wherein the digital adaptive equalizer comprises a feed forward equalizer, a three-level data slicer and a decision feedback equalizer.

223. (New) The computer network device according to claim 222, wherein the digital adaptive equalizer comprises an adder that has a first input, a second input and an output, wherein the first input is coupled to the feed forward equalizer, wherein the second input is coupled to the decision feedback equalizer and wherein the output is coupled to the three-level data slicer.

224. (New) The computer network device according to claim 222, wherein first receiver

and equalizer comprises timing recovery circuitry, wherein timing recover circuitry comprises a low gain error generator, a high gain error generator, a loop filter, a phase inverter and a controller.